Assignment 4: Question 4.1

\* Project : Assignment 4

\* Name of the file : COA\_A4\_P1.S

\* Brief Description of file : Assembly code to implement a double layered page table while illustrating privilege levels for pages of size 2 MB

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We implement 2 MB sized pages, which is greater than 10kB as the question requires. We thus take the information imparted in the lab session and apply it on 2 MB pages.

The page table has been created to identically map the virtual address to physical address

The linker loads the code at 0x10010000 and we use this knowledge to set page table accordingly.

We first load sp value and machine trap handler addresses.

We now access the address values which we require on the page walk.

Following the address calculations and right shift as mentioned in the RISC V specifications, we set pmp addresses and pmp configuration values, which enables the physical memory protection, i.e. pmp.

After this, we switch privilege levels from machine to supervisor mode, wherein we set satp with the root page table address and mode as 8.

Successful execution of instructions after this demonstrates the page table creation.

We show that the machine mode code is inaccessible from supervisor mode by attempting and failing to jump from supervisor to machine mode thus causing an instruction access fault, as the supervisor mode code is accessible from both levels whereas machine mode code is only accessible from machine mode.

The specifics of which functionality of the above explanation is done and where is shown via comments in the assembly code file.